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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,158	10/01/2003	Ming-Fang Wang	67,200-1160	8159

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EXAMINER	
GEORGE, PATRICIA ANN	
ART UNIT	PAPER NUMBER
1765	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,158	WANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 9, 13, 15, 19, and 21 are rejected under 35 U.S.C. 103(a) as being over Fujii et al. (5,644,158), in view of Jeon (2003/0194853), and evidenced by Chao (4,906,589) and Weber et al. (5,075,641).

As to claims 1 and 19, Fujii et al. teaches a method for treating a gate structure comprising a high-k dielectric layer (see col.1, para. 1) over a semiconductor sunstrate (abstract), to reduce the surface density of the gate insulator (i.e. dielectric) beneath the

electrode (col.4, line 38-50), to lower the leakage current (i.e. interference states between gate dielectric and electrode) (see col.3, lines 25-45).

Fujii et al teaches to form a gate structure (see col. 4, lines 1 –10), however Fujii is silent as to the gate structures lithography patterned and etched.

Chao (4,906,589) provides evidence that it is well known that gate structures are lithography patterned and etched.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to implore the steps of lithography patterning and etching gate structures, as Choa, to modify the method of forming a gate structure, as Fujii et al., because Fujji et al.'s silence shows and absence of criticality in the method implored, and Choa provides evidence that it is well known and functional to do so. In absence of unexpected results, one skilled in the art would be motivated to use well known and functional methods, as it saves time and cost saving to do so.

Fujii et al. teaches the provision of a hydrogen and nitrogen anneal treatment (see col. 4, lines 37 –50), as in claims 1, 9, 13, 15, and 19.

After the forming of the gate structure, and before the anneal treatment, Fujii et al. teaches forming a thin film capacitance layer using a sputtering method (i.e. at least one plasma treatment comprising source gas N2 gate structure following the formation of the gate structure).

Although Fujii et al. teaches at least one plasma treatment (i.e. sputtering method), and it is known that sputtering methods typically use a source gas N2, Fujii et

al. is silent as to the sputter plasma source gas N2. (Examiner interprets treatment to mean subjection to some agent or action.)

Weber et al. provides evidence that sputter nitrogen plasma is typical, known, and effective (see col. 11, lines 46-60).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming a gate structure, as Fujii et al., to include the plasma source gas is N2, as applicants' limitation of claims 1 and 19, because Fujji et al.'s silence shows and absence of criticality in the method implored, and Weber et al. provides evidence that it is typical, known, and functional to do so. In absence of unexpected results, one skilled in the art would be motivated to use typically known, functional methods, as it saves time and cost saving to do so.

Fujii et al. fails to teach the high-k layer is a stack.

Jeon teaches use of a treated high-k gate stack, as applicants' limitation (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of forming a gate structure, as Fujii et al., to include high-k dielectric layer is a stack, as applicants' limitation, because Jeon teaches such methods of use of integrated stacked gate dielectrics overcome the known problem of oxidation of silicon by certain high-K dielectric materials when the high-K dielectric material is formed directly on a silicon substrate by using a method of forming

a treated high-K dielectric stack either overcomes or takes advantage of such reactions, and provides electrical advantages of a higher K.

As to claim 2, Fujii et al teaches anneal at steps 4 and 6, both after step 2, the plasma treatment (i.e. sputter).

As claim 13 is the combination of the limitations in claims 1 and 2, all limitations have been addressed in the discussion above.

As claim 21 only rearranges limitations already presented in claim 1, all limitations have been addressed in the discussion above.

Claim Rejections - 35 USC § 103

Claims 3, 14, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al, and Jeon as applied to claims 1, 2, 13, 19, and 21 above, further in view of Powell et al. (6,458,714) .

The teaching of Fujii et al. fails to teach the temperature limitations presented in claims 3, 14, and 22.

Powell teaches a step of annealing the gate electrode structure at 600 degrees C. to 100 degrees C. which encompasses applicants range of 600 to 750 degree C, as in claims 3, 14, and 22 (see col. 7, lines 50-67).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the step of annealing, as Powell et al., when forming a

high-K dielectric stacked gate structure, as Fijii et al., because Powell et al. teaches the anneal will protect underlying layers.

Claim Rejections - 35 USC § 103

Claims 4, and 15, rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al, and Jeon as applied to claims 1, 2, 13, 19, and 21 above, further in view of Wolf (Silicon Processing for the VLSI Era, Volume 1; Process Technology; pg.58, para. 2, 1986 Latice Press; ISBN 0-9616721-3-7).

The teaching of Fujii et al. fails to teach the gas limitation presented in claims 4, and 15.

Wolf teaches it is desirable to use N2 ambient for annealing (as in claims 4 and 15).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of annealing after forming and treating the gate structure (para. 0016), as Fujii et al., by including the temperature range and N2 ambient, as Wolf, because Wolf teaches it is known and a desirable option of annealing.

Claim Rejections - 35 USC § 103

Claims 5, 7, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al, and Jeon as applied to claims 1, 2, 13, 19, and 21 above, further in view of Shinriki et al. (2005/0074983).

The modified teaching of Fujii et al. is silent as to the base dielectric layer of the gate stack comprising SiO.sub.2, as in claims 5.

Shinriki et al. teaches it is preferably to change the composition of the dielectric stack gradually from the SiO.sub.2 base to a composition primarily of high-k dielectric, metal oxides such as hafnium oxide (see para. 83) as to avoid defects such as interface states (see para. 0006), as in claims 5, 7, 16, and 18.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the teaching of a dielectric stack layer, as in Fujii et al., to include that the base comprise SiO.sub.2, under hafnium oxide, as in Shinriki et al., because Shinriki et al. teaches it is preferable because it avoids defects such as interface states (see para. 0006).

Claim Rejections - 35 USC § 103

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al, and Jeon as applied to claims 1, 2, 13, 19, and 21 above, further in view of Haukka et al. (2002/0115252).

Fujii et al. is silent as to the materials listed in claim 6, being high-k.

Haukka et al. teaches it is known that high-k materials comprise all the materials as claimed by applicants' in claim 6 (see para. 7).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the high-k materials, as listed by applicatnts, when forming a stacked gate structure of high-K dielectric materials, as Fujii et al., because

Haukka et al. teaches it is known that claimed materials are high-K dielectrics, and Fujii et al. teaches process improvement result as an effect of using high-K materials.

Claim Rejections - 35 USC § 103

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified invention of Fujii et al, Jeon, and Shinriki, as applied to claims 5, 7, 16, and 18 above, and further in view of Sarigiannis et al. of 2004/0152304.

As to claim 8, the modified invention of Fujii et al. is silent as to how the high-k dielectric materials may be formed, such as ALD (ALCVD) at less than 300 degree C, as in claim 8.

Sarigiannis et al.teaches an ALD deposition temperature of 200 degree C, (para.4, l.11), which is within the claimed range of less than about 300 degree C".

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a process temperature for ALD deposition, as Sarigiannis, when forming the gate structure, of Fujii et al., because Sarigiannis teaches it can be advantageous.

Claim Rejections - 35 USC § 103

Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al, and Jeon as applied to claims 1, 2, 13, 19, and 21 above, further in view of Lamont, Jr. (4,457,825).

As for claim 11, the modified invention of Fujii is silent as to the pressure of the plasma treatment, as applicants' claim.

Lamont, Jr. teaches typical operation of sputter can occur in a range of between about 1 mTorr to about 100 mTorr which overlaps applicants claimed range of about 100 mTorr to about 10 Torr (see col. 8. line 46).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of Fujii et al. to include the pressure ranges, as in Lamont, Jr., because Lamont Jr. teaches such a range used at the pressure as applicants' limitations in claim 11 and 20, are known to be effective. Since the reference of Lamont, Jr. does not limit the pressure range selected, one of ordinary skill would use a plasma etcher for the method of plasma treatment at any desired pressure, including applicants specifically claimed range.

Response to Arguments

The remarks toward the reference of Fujii et al. (6,596,599) not proper under 103(c) filed on 12/25/2006 is sufficient to overcome the 103(a) reference. A new grounds of rejection is offered above.

Applicants' copy and paste two paragraphs, on page 17, from the reference of Shinriki, however fails to discuss the relevance of these to paragraphs to use of Shinriki as prior art. Applicant fail to provide evidence of how the reference of Shinrike fails as a 35 USC 103 reference.

Applicants' remarks on pages 19, 20, and 21 toward proper motivation to combine fail to present anything specific about the motivation which is defective. Because applicants' do not provide evidence that the motivations are lacking, examiner have no response.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571) 272-5955. The examiner can normally be reached on Tues. - Sat. between 8:00 am and 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAG/ 03/07

Patricia A George
Examiner
Art Unit 1765

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER